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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,240	04/13/2006	Masamichi Nogami	285366US2PCT	3473
22850	7590	01/07/2009		
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER YAM, STEPHEN K	
			ART UNIT	PAPER NUMBER
			2878	
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			01/07/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b> 10/566,240	<b>Applicant(s)</b> NOGAMI ET AL.	
	<b>Examiner</b> STEPHEN YAM	<b>Art Unit</b> 2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10 is/are rejected.
- 7) ☒ Claim(s) 9 and 11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 March 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>1/3/06, 5/23/08</u> . | 6) <input type="checkbox"/> Other: ____.  |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 1 and 8 are objected to because of the following informalities:

In Claim 1, line 7, "a series circuit" lacks proper antecedent basis as the term is already defined.

In Claim 8, line 10, "econd" should be replaced with "second".

2. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagisawa JP 2000-315923.

Regarding Claims 1 and 6, Yanagisawa teaches (see Fig. 1) a gain switching circuit that switches a conversion gain of a preamplifier (2), the preamplifier outputting a voltage signal by amplifying an output current of a photo-detecting element (1) that converts a burst optical signal into an electrical signal (see Paragraph 0015), the preamplifier being configured with a series circuit formed with a first resistor (R3) and a first switching element (TR1) and a series circuit formed with a second resistor (R4) and a second switching element (TR2) respectively connected in parallel with a feedback resistor (R1) (see Fig. 1), the gain switching circuit inputting a first

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gain switching period (see Fig. 3) for switching to a first conversion gain and a second gain switching period for switching to a second conversion gain (see Fig. 3 and Paragraph 0015) from outside upon receiving an output from the preamplifier (see Fig. 1), the gain switching circuit comprising: a first operating unit (3, 5) that generates a first switching element operating signal (from (5) to (TR1)) for closing the first switching element within the first gain switching period; and a second operating unit (4, 6) that generates a second switching element operating signal (from (6) to (26)) for closing the second switching element within the second gain switching period.

Regarding Claims 2 and 7, Yanagisawa teaches the first gain switching period is different from the second gain switching period (See Fig. 3).

Regarding Claim 3, Yanagisawa teaches closing of the second switching element by the second operating unit within the second gain switching period is enabled after the first switching element is closed by the first operating unit within the first gain switching period (See Fig. 3).

Regarding Claim 4, Yanagisawa teaches the first operating unit outputs the first switching element operating signal, when an output level of the preamplifier exceeds a first discrimination level (V1), if a timing when the output level exceeds the first discrimination level exceeds is within the first gain switching period (see Fig. 3), and the second operating unit outputs the second switching element operating signal, when the output level of the preamplifier exceeds a second discrimination level (V2), if the first switching element operating signal has been output, and if a timing when the output level exceeds the second discrimination level is within the second gain switching period (See Fig. 3).

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Regarding Claim 8, Yanagisawa teaches (See Fig. 2, 4) the first switching element operating signal is generated using a first discrimination level (V2) and the second switching element operating signal is generated using a second discrimination level (V3), the gate generating circuit generates the gate signal based on a third discrimination level (V1) that satisfies  $V10 < V1$  and  $V10 < V2$  where V1 is the first discrimination level, V2 is the second discrimination level, and V10 is the third discrimination level.

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagisawa.

Regarding Claim 5, Yanagisawa teaches the device in Claim 4, according to the appropriate paragraph above. Yanagisawa does not teach a particular relation for the first and second discrimination levels and the lowering of a gain of the preamplifier. It is well known in the art to determine optimal relationships between operating parameters of the system. it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the claimed relation range for the first and second discrimination levels and the lowering of a gain of the preamplifier, in the device of Yanagisawa, since it has been held that where the

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general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding Claim 10, Yanigasawa teaches the device in Claim 7, according to the appropriate paragraph above. Yanigasawa also teaches embodiments with two discrimination levels (see Fig. 1) and three discrimination levels (see Fig. 4). Yanigasawa does not teach the circuit with four discrimination levels. It is well known in the art to provide continuing components in a system, to provide even further refinement of the operation of the system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide four discrimination levels (as opposed to merely two or three as taught in Yanigasawa), in the device of Yanigasawa, to further improve the gain characteristics and operation of the preamplifier for optimal signal output.

#### ***Allowable Subject Matter***

7. Claims 9 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 9, the invention as claimed, specifically in combination with the gate generating circuit includes a counter circuit that generates a clock signal, and the gate generating circuit generates a gate signal having a time width of a predetermined number of clocks by using

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the clock signal generated by the counter circuit, is not disclosed or made obvious by the prior art of record.

Regarding Claim 11, the invention as claimed, specifically in combination with the gate generating circuit generates a logical product signal of a first basic gate signal that is generated by the first variation-point detecting circuit with a time width of a predetermined variation point count length and a second basic gate signal that is generated by the second variation-point detecting circuit with a time width of a predetermined variation point count length as the gate signal, is not disclosed or made obvious by the prior art of record.

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Doh et al. US 6,911,644, Doh et al. US 6,909,082, Doh et al. US 7,218,865, and Mohandas et al. US 6,933,786 teach similar amplifiers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN YAM whose telephone number is (571)272-2449.

The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen Yam/  
Primary Examiner, Art Unit 2878